Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1-16. (Canceled).

17. (Currently Amended) A system to process ~~instruction sequences all having the same predetermined sequence bit length~~ very long instruction words (VLIWs), the system comprising:

a decode unit to decode an instruction of ~~an instruction sequence~~ a VLIW received during an instruction fetch, wherein all instructions of the ~~instruction sequence~~ VLIW have the same predetermined instruction bit length; and

first and second processing channels, each processing channel including a plurality of functional units, at least one of the functional units of each processing channel being a data processing unit and at least one other of the functional units of each processing channel being a memory access unit;

wherein the decode unit is operable to determine whether the instruction defines a single operation or two independent operations and to control the first and second processing channels based on the determination.

18. (Previously Presented) The system according to claim 17, wherein, when the decode unit determines that the instruction defines two independent operations, the decode unit is operable to control the first channel to implement one of the two independent operations and the second channel to implement the other of the two independent operations, and wherein the first and second channels execute their respective independent operations simultaneously.

19. (Previously Presented) The system according to claim 17, wherein, when the decode unit determines that the instruction defines a single operation, the decode unit is operable to control the first and second processing channels to cooperate to execute the single operation.

20. (Previously Presented) The system according to claim 17, wherein the first and second processing channels share at least one common register file and are capable of simultaneously accessing the at least one common register file.

21. (Previously Presented) The system according to claim 17, wherein the decode unit is operable to determine whether the instruction defines a single operation or two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction.

22. (Previously Presented) The system according to claim 21, wherein the instruction has a length of n bits, and the at least one predetermined bit location includes the n/2th bit and the nth bit.

23. (Previously Presented) The system according to claim 21, wherein the decode unit is operable to identify certain combinations of the two independent operations based on the at least one identification bit, and wherein a first combination denotes two data processing operations, a second combination denotes two memory access operations, a third combination denotes a data processing operation and a memory access operation, and a fourth combination denotes a long instruction.

24. (Currently Amended) A method of operating a system that processes ~~instruction sequences all having the same predetermined sequence bit length~~ very long instruction words (VLIWs), each instruction of ~~an instruction sequence~~ a VLIW having the same predetermined instruction bit length, the method comprising:

decoding an instruction of the ~~instruction sequence~~ VLIW received during an instruction fetch to determine whether the instruction defines a single operation or two independent operations;

when the instruction defines two independent operations, supplying one of the independent operations to a first processing channel having a first plurality of functional units including a first data processing unit and a first memory access unit, and supplying

the other of the independent operations to a second processing channel having a second plurality of functional units including a second data processing unit and a second memory access unit, wherein the two independent operations are executed simultaneously; and

when the instruction defines a single operation, controlling the first and second processing channels to cooperate to execute the single operation.

25. (Previously Presented) The method according to claim 24, wherein decoding the instruction includes determining whether the instruction defines the single operation or the two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction.

26. (Previously Presented) The method according to claim 25, wherein determining whether the instruction defines the single operation or the two independent operations includes determining whether the instruction defines the single operation or the two independent operations based on the at least one identification bit that indicates the nature of the two independent operations when the instruction defines the two independent operations.

27. (Previously Presented) The method according to claim 25, wherein determining whether the instruction defines the single operation or the two independent operations is based on an n/2th bit and an nth bit of the instruction having n bits.

28. (Currently Amended) An article comprising a medium for storing commands to enable a processor-based system to:

process very long instruction word data including ~~instruction sequences all having the same predetermined sequence bit length~~ very long instruction words (VLIWs), each instruction of ~~an instruction sequence~~ a VLIW having the same predetermined instruction bit length, wherein the commands to enable the processor-based system to process the very long instruction word data include commands to enable the processor-based system to decode an instruction of the ~~instruction sequence~~ VLIW

received during an instruction fetch to determine whether the instruction defines a single operation or two independent operations;

when the instruction defines two independent operations, supply one of the independent operations to a first processing channel and supply the other of the independent operations to a second processing channel, wherein the two independent operations are executed simultaneously; and

when the instruction defines a single operation, control the first and second processing channels to cooperate to execute the single operation.

29. (Previously Presented) The article according to claim 28, wherein the commands to enable the processor-based system to decode the instruction include the commands to enable the processor-based system to decode the instruction to determine whether the instruction defines the single operation or the two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction.

30. (Previously Presented) The article according to claim 29, wherein the commands to enable the processor-based system to decode the instruction include the commands to enable the processor-based system to decode the instruction to determine whether the instruction defines the single operation or the two independent operations based on the at least one identification bit that indicates the nature of the two independent operations when the instruction defines the two independent operations.

31. (Previously Presented) The article according to claim 29, wherein the commands to enable the processor-based system to decode the instruction include the commands to enable the processor-based system to decode the instruction to determine whether the instruction defines the single operation or the two independent operations based on an n/2th bit and an nth bit of the instruction having n bits.

32. (Currently Amended) A method of operating a system that processes ~~instruction sequences all having the same predetermined sequence bit length~~ very long instruction words (VLIWs), each instruction of ~~an instruction sequence~~ a VLIW having the same

predetermined instruction bit length and at least one identification bit at at least one predetermined bit location in the instruction, the method comprising:

fetching the ~~instruction sequence~~ VLIW from a program memory;

decoding each instruction of the ~~instruction sequence~~ VLIW, wherein decoding each instruction includes reading the identification bit of each instruction to determine:

a) whether the instruction defines a single operation or two independent operations, and

b) when the instruction defines two independent operations, the nature of each of the two independent operations selected at least from a data processing category of operation and a memory access category of operation.

33. (Currently Amended) An article comprising a medium for storing commands to enable a processor-based system to:

process very long instruction word data including ~~instruction sequences all having the same predetermined sequence bit length~~ very long instruction words (VLIWs), each instruction of ~~an instruction sequence~~ a VLIW having the same predetermined instruction bit length and at least one identification bit at at least one predetermined bit location in the instruction, wherein the commands to enable the processor-based system to process the very long instruction word data include commands to enable the processor-based system to decode an instruction of the ~~instruction sequence~~ VLIW received during an instruction fetch to determine:

a) whether the instruction defines a single operation or two independent operations, and

b) when the instruction defines two independent operations, the nature of each of the two independent operations selected at least from a data processing category of operation and a memory access category of operation.